CLAIMS

1. A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions, the method comprising steps of:

(A) identifying the position of a bit in a set of *n* consecutive defective bits in the memory;

(B) generating an entry in a shift redundancy record indicating that the bit identified in step (A) is defective; and

(C) generating a hint record indicating the number *n* of bits in the set of consecutive defective bits.

2. The method of claim 1, wherein $n=1$.

3. The method of claim 1, wherein $n=2$.

4. The method of claim 1, wherein step (A) comprises a step of identifying a defective bit that is adjacent to a functional bit in the memory; and wherein the method further comprises a step of:

(D) performing steps (A)-(C) for a plurality of sets of consecutive defective bits in the memory.

5. The method of claim 1, wherein the step (B) comprises a step of generating a single-bit entry in the shift redundancy record indicating that the bit identified in step (A) is defective.

6. The method of claim 1, wherein the memory further comprises a plurality of input/output ports for accessing the plurality of bits, and wherein the method further comprises steps of:

(D) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from the input/output ports.

7. The method of claim 1, wherein step (C) comprises a step of generating a hint record representing the value *n*-1.

8. A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions and a plurality of input/output ports for accessing the plurality of bits, the method comprising steps of:

(A) identifying the position of a bit in a set of *n* consecutive defective bits in the memory, wherein the identified is adjacent to a functional bit in the memory;

(B) generating a single-bit entry in a shift redundancy record indicating that the bit identified in step (A) is defective;

(C) generating a hint record representing the value *n*-1;

(D) performing steps (A)-(C) for a plurality of sets of consecutive bits in the memory; and

(E) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from the input/output ports.

9. An apparatus for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions, the apparatus comprising:

means for identifying the position of a bit in a set of *n* consecutive defective bits in the memory;

means for generating an entry in a shift redundancy record indicating that the bit identified in step (A) is defective; and

means for generating a hint record indicating the number *n* of bits in the set of consecutive defective bits.

10. The apparatus of claim 9, wherein the means for generating comprises means for generating a single-bit entry in the shift redundancy record indicating that the bit identified by the means for identifying is defective.

11. The apparatus of claim 9, wherein the memory further comprises a plurality of input/output ports for accessing the plurality of bits, and wherein the apparatus further comprises:

means for controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports.

12. The apparatus of claim 9, wherein the means for generating comprises means for generating a hint record representing the value *n*-1.

13. A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the method comprising steps of:

(A) selecting a first value for a current shift redundancy record variable, wherein the current shift redundancy record value may be toggled between the first value and a second value;

(B) for each of a plurality of consecutive values of i, performing steps of:

(1) if bit b[i] is defective and bit b[i-1] is functional, performing steps of:

(a) toggling the value of the current shift redundancy record variable;

(b) identifying a set of *n* consecutive defective bits including bit b[i];

(c) storing a hint value in a hints record entry corresponding to bit b[i], the hint value indicating the number *n*; and

(2) storing the current shift redundancy record value in a shift redundancy record element corresponding to bit b[i].

14. The method of claim 13, wherein $n=1$.

15. The method of claim 13, wherein $n=2$.

16. The method of claim 13, wherein the step (B)(2) comprises a step of storing a single-bit value in the shift redundancy record representing the position of bit b[i].

17. The method of claim 13, wherein the step (B)(1) further comprises a step of:

(B)(1)(d) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports of the memory.

18. The method of claim 13, wherein the hint value is equal to *n*-1.

19. A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the method comprising steps of:

(A) selecting a first value for a current shift redundancy record variable, wherein the current shift redundancy record value may be toggled between the first value and a second value;

(B) for each of a plurality of consecutive values of i, performing steps of:

(1) if bit b[i] is defective and bit b[i-1] is functional, performing steps of:

(a) toggling the value of the current shift redundancy record variable;

(b) identifying a set of *n* consecutive defective bits including bit b[i];

(c) storing a hint value representing the value *n*-1 in a hints record entry corresponding to bit b[i];

(d) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports of the memory; and

(2) storing the current shift redundancy record value in a single-bit shift redundancy record element corresponding to bit b[i].

20. An apparatus for use in a computer system including a memory, the memory including a plurality of bits at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the apparatus comprising:

means for selecting a first value for a current shift redundancy record variable, wherein the current shift redundancy record value may be toggled between the first value and a second value;

for each of a plurality of consecutive values of i:

means for toggling the value of the current shift redundancy record variable if bit b[i] is defective and bit b[i-1] is functional;

means for identifying a set of *n* consecutive defective bits including bit b[i] if bit b[i] is defective and bit b[i-1] is functional; and

means for storing a hint value in a hints record entry corresponding to bit b[i], the hint value indicating the number *n*; and

means for storing the current shift redundancy record value in a shift redundancy record element corresponding to bit b[i].

21. The apparatus of claim 20, wherein the means for the current shift redundancy record value comprises means for storing a single-bit value in the shift redundancy record representing the position of bit b[i].

22. The apparatus of claim 20, further comprising:

means for controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports of the memory.

23. A computer system comprising:

a memory comprising a plurality of bits and a plurality of input/output ports for accessing the plurality of bits;

a memory defect map specifying positions of defective ones of the plurality of bits; and

a shift encoder for encoding positions of defective ones of the plurality of bits in a shift encoding, the shift encoding comprising:

a shift redundancy record representing positions of transitions between functional bits and defective bits in the memory; and

a hints record representing numbers of bits in sets of consecutive defective bits in the memory.

24. The method of claim 23, wherein the shift redundancy record comprises a plurality of shift redundancy record elements corresponding to the plurality of input/output ports.

25. The method of claim 24, wherein each of the plurality of shift redundancy record elements comprises a single-bit value.

26. The method of claim 23, wherein the number of bits in the hints record is equal to H, wherein the value of H is given by the following equation:

$$H = \sum_{j=0}^{N-2} \text{ceil}(\log_2(N-j)) ,$$

wherein N is a maximum permitted number of consecutive defective bits in the memory, and wherein the ceil() function rounds up its single argument to the closest integer.

27. A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits and a plurality of input/output ports for accessing the plurality of bits, the method comprising steps of:

(A) receiving a shift encoding that encodes positions of defective ones of the plurality of bits, the shift encoding comprising:

a shift redundancy record that encodes transitions between functional bits and defective bits in the memory; and

a hints record that encodes numbers of bits in sets of consecutive defective bits in the memory; and

(B) generating, based on the shift encoding, a plurality of shift values that specify mappings between the plurality of input/output ports and corresponding ones of the plurality of bits.

28. The method of claim 27, wherein the plurality of bits have a plurality of consecutive positions within the memory, wherein b[i] refers to the bit at position i in the memory, wherein the hints record comprises at least one hints record element, and wherein step (B) comprises steps of:

(B)(1) identifying a position i for which bit b[i] is defective and bit b[i-1] is functional;

(B)(2) identifying a hints record element in the hints record that corresponds to bit b[i]; and

(B)(3) generating a select one of the plurality of shift values based on the hints record element identified in step (B)(2).

29. The method of claim 28, wherein the hints record element identified in step (B)(2) has a hint value, and wherein the step (B)(3) comprises a step of assigning the hint value plus one to the select one of the plurality of shift values.

30. The method of claim 28, wherein the hints record element identified in step (B)(2) has a hint value, wherein the step (B) further comprises a step of identifying a previous shift value, and wherein the step (B)(3) comprises a step of assigning the previous shift value plus the hint value plus one to the select one of the plurality of shift values.

31. The method of claim 27, wherein the shift redundancy record includes a plurality of shift redundancy values, wherein SRP[i] refers to a shift redundancy value having index i in the plurality of shift redundancy values, and wherein the step (B) comprises steps of:

(1) selecting an initial shift value for a default shift variable;

(2) selecting as a current hints record element an initial hints record element having an initial hint value;

(3) for each of a plurality of consecutive values of i, performing steps of:

(a) if SRP[i] is not equal to SRP[i-1], performing steps of:

(i) adding one plus a value of the current hints record element to the value of the default shift variable to produce a new value for the default shift variable; and

(ii) selecting as the current hints record element a next hints record element having a next hint value; and

(b) generating a shift value in the plurality of shift values that is equal to the value of the default shift variable.

32. The method of claim 27, wherein the number of bits in the hints record is equal to H, wherein the value of H is given by the following equation:

$$H = \sum_{j=0}^{N-2} \text{ceil}(\log_2(N-j)) ,$$

wherein N is a maximum permitted number of consecutive defective bits in the memory, and wherein the ceil() function rounds up its single argument to the closest integer.

33. A computer system comprising:

a memory comprising a plurality of bits and a plurality of input/output ports for accessing the plurality of bits, wherein IO[i] refers to an input/output port at position i;

a plurality of stored shift redundancy record signals representing shift values for the plurality of I/O ports, wherein SRP[i] refers to a shift redundancy record signal for input/output port IO[i];

a stored hints record signal representing the number of bits in a set of consecutive defective bits in the memory;

a first multiplexer comprising a first data input receiving the stored hints record signal, a second data input receiving a signal R0[i-1], a selection input receiving signal SRP[i], and an output providing a signal R1[i]; and

a second multiplexer comprising a first data input receiving a signal having a predetermined voltage level, a second data input receiving signal R0[i-1], a selection input receiving SRP[i], and an output providing a signal R0[i].

34. The computer system of claim 33, wherein the predetermined voltage level comprises a high logical voltage level.

35. The computer system of claim 33, further comprising:

a first inverter comprising an input receiving signal R0[i] and an output providing a first inverted signal;

a second inverter comprising an input receiving signal R1[i] and an output providing a second inverted signal;

a first NAND gate comprising a first input coupled to the output of the first inverter, a second input coupled to the output of the second inverter, and an output providing a first NAND signal;

a second NAND gate comprising a first input receiving signal R0[i], a second input coupled to the output of the second inverter, and an output providing a second NAND signal;

a third inverter coupled to the output of the first NAND gate and an output providing a signal SHIFT0;

a fourth inverter coupled to the output of the second NAND gate and an output providing a signal SHIFT1; and

a fifth inverter coupled to the output of the third NAND gate and an output providing a signal SHIFT2.

36. The computer system of claim 33, wherein the number of bits in the stored hints record signal is equal to H, wherein the value of H is given by the following equation:

$$H = \sum_{j=0}^{N-2} \text{ceil}(\log_2(N-j)) ,$$

wherein N is a maximum permitted number of consecutive defective bits in the memory, and wherein the ceil() function rounds up its single argument to the closest integer.